Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**10.1" SD+ 16:9 Color TFT-LCD**
Model Name	B101EW01 V1
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
All	7/29/2009	Howard Lee	7/29/2009
Checked & Approved by	**Date**	**Prepared by**	
		Carol Tang	7/29/2009

Note: This Specification is subject to change without notice.

NBBU Marketing Division /
AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/12/29	All	First Edition for Customer		
1.0 2008/3/27	All	Final Edition		
2.0 2009/05/07	26	HW control table [Radium IC]	HW control table [Novatek IC]	
	27	Carton Package (1 layer)	Carton Package (2 layer)	
2.1 2009/07/29	28~31	EDID checksum 9B	EDID checksum C3	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101EW01 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support 1280(H) x 720(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B101EW01 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

<table>
<tr><th>Items</th><th>Unit</th><th>Specifications</th></tr>
<tr><td>Screen Diagonal</td><td>[mm]</td><td>255.54(10.1W")</td></tr>
<tr><td>Active Area</td><td>[mm]</td><td>222.72(H) X 125.28(V)</td></tr>
<tr><td>Pixels H x V</td><td></td><td>1280x3(RGB) x 720</td></tr>
<tr><td>Pixel Pitch</td><td>[mm]</td><td>0.1740 (H) x 0.1740 (V)</td></tr>
<tr><td>Pixel Arrangement</td><td></td><td>R.G.B. Vertical Stripe</td></tr>
<tr><td>Display Mode</td><td></td><td>Normally White</td></tr>
<tr><td>White Luminance
Note: I_{LED} is LED current</td><td>[cd/m^2]</td><td>180 typ
(Note1)</td></tr>
<tr><td>Luminance Uniformity (5P)</td><td></td><td>1.25 max</td></tr>
<tr><td>Contrast Ratio</td><td></td><td>500 typ</td></tr>
<tr><td>Response Time</td><td>[ms]</td><td>16 typ</td></tr>
<tr><td>Nominal Input Voltage VDD</td><td>[Volt]</td><td>+3.3 typ.</td></tr>
<tr><td>Power Consumption</td><td>[Watt]</td><td><table><tr><th>Typ</th><th>Max</th><th>Note</th></tr><tr><td>2.7W</td><td>2.9W</td><td>Type I , V_{in} =12V</td></tr><tr><td>3.1W</td><td>3.3W</td><td>Type I , V_{in} =5V</td></tr></table>@ Black pattern</td></tr>
<tr><td>Weight</td><td>[Grams]</td><td>175 max.</td></tr>
<tr><td>Physical Size
(w/ bracket & PCBA)</td><td>[mm]</td><td><table><tr><th></th><th>L</th><th>W</th><th>T</th></tr><tr><td>Max</td><td>243.5</td><td>147.0</td><td>3.6</td></tr><tr><td>Typical</td><td>243.0</td><td>146.5</td><td></td></tr><tr><td>Min</td><td>242.5</td><td>146.0</td><td>-</td></tr></table></td></tr>
<tr><td>Electrical Interface</td><td></td><td>1 channel LVDS</td></tr>
</table>

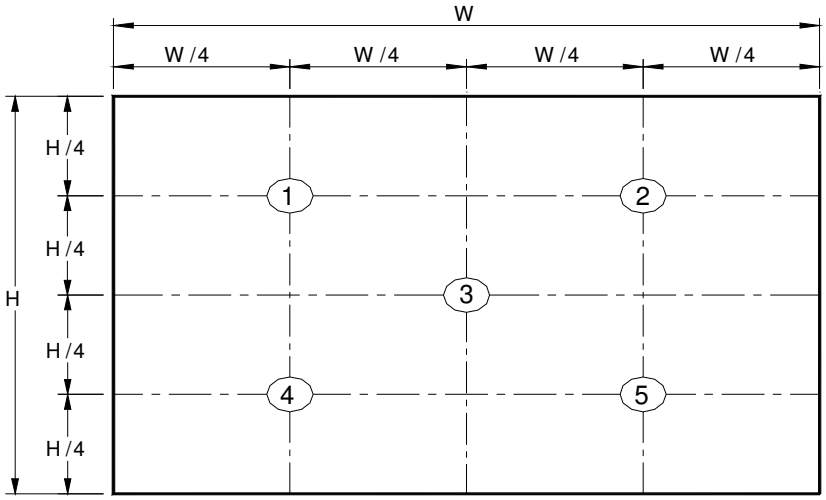
Glass Thickness	[mm]	0.5
Surface Treatment		Anti-Glare
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

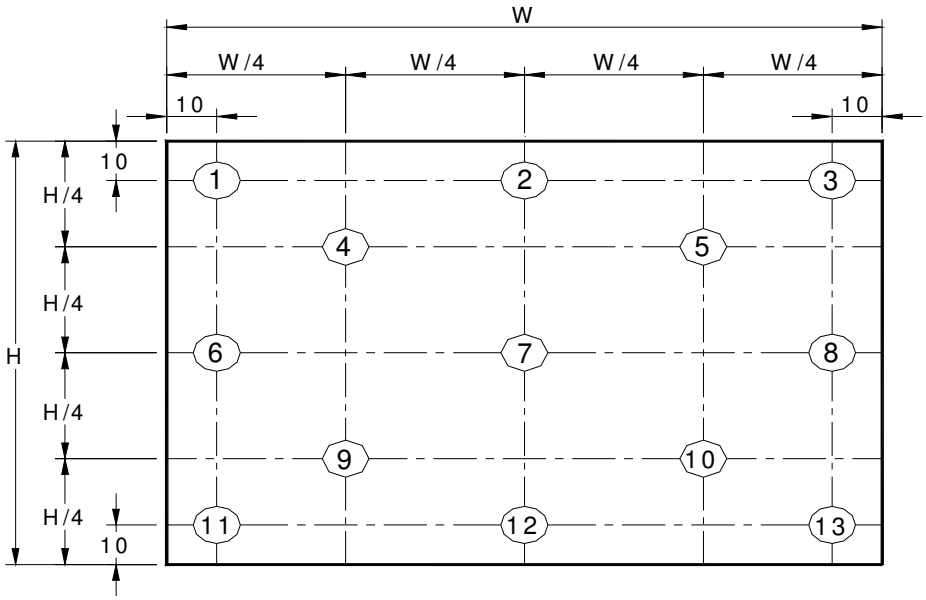
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance **ILED=20mA**			5 points average	**153**	**180**	**-**	cd/m^2	1, 4, 5
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	**40** **40**	**45** **45**	**-** **-**	degree	4, 9
		ϕ_H ϕ_L	Vertical (Upper) CR = 10 (Lower)	**10** **30**	**15** **35**	**-** **-**		
Luminance Uniformity		δ_{5P}	5 Points	**-**	**-**	**1.25**		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	**-**	**-**	**1.60**		2, 3, 4
Contrast Ratio		**CR**		**400**	**500**	**-**		4, 6
Cross talk		**%**				**4**		4, 7
Response Time		**T_r**	Rising	**-**	**12**	**-**	msec	4, 8
		T_f	Falling	**-**	**4**	**-**		
		T_{RT}	Rising + Falling	**-**	**16**	**-**		
Color / Chromaticity Coodinates	**Red**	**Rx**	CIE 1931	**0.551**	**0.581**	**0.611**		4
		Ry		**0.307**	**0.337**	**0.367**		
	Green	**Gx**		**0.302**	**0.332**	**0.362**		
		Gy		**0.545**	**0.575**	**0.605**		
	Blue	**Bx**		**0.130**	**0.160**	**0.190**		
		By		**0.108**	**0.138**	**0.168**		
	White	**Wx**		**0.283**	**0.313**	**0.343**		
		Wy		**0.299**	**0.329**	**0.359**		
NTSC		**%**		**-**	**45**	**-**		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



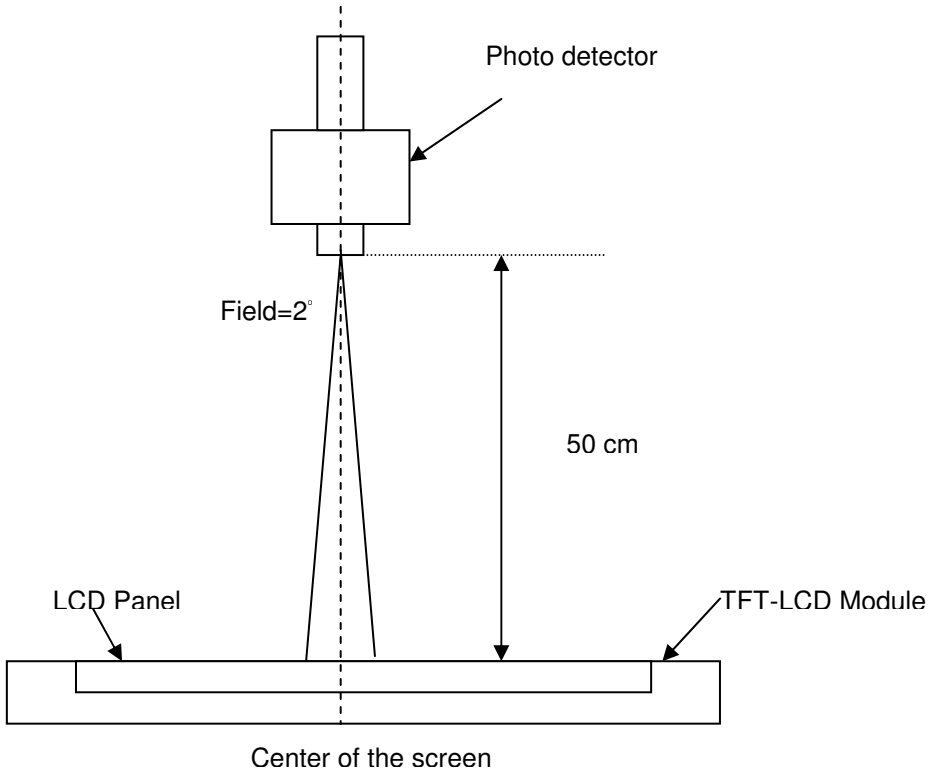
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

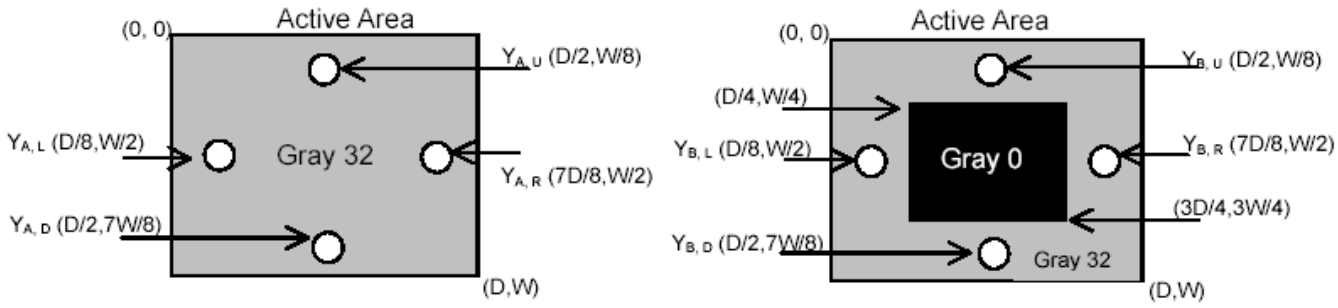
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

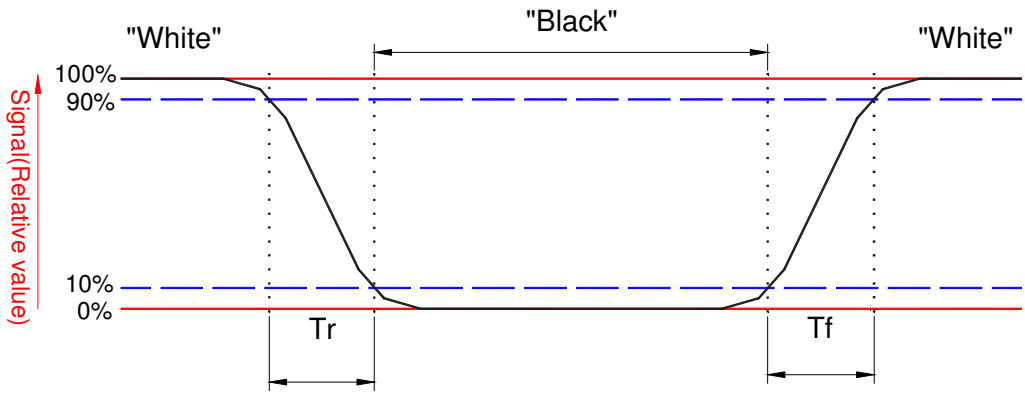
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



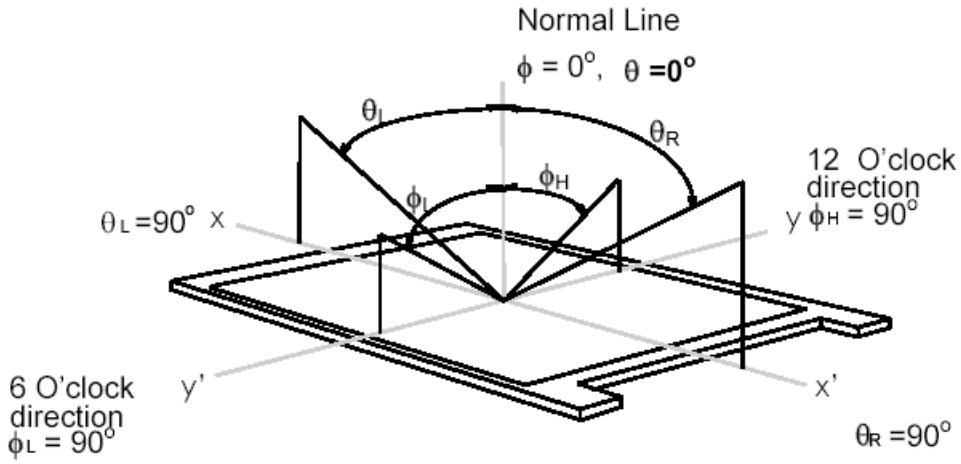
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



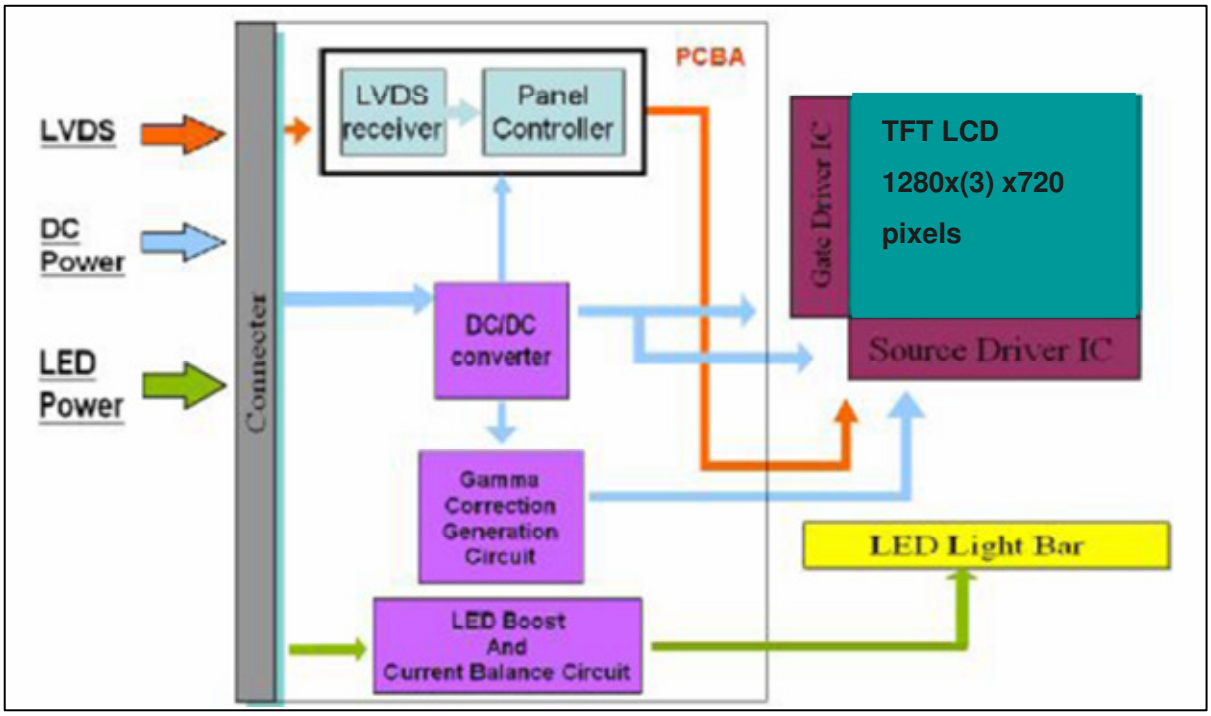
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin (One ch/connector Module).



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

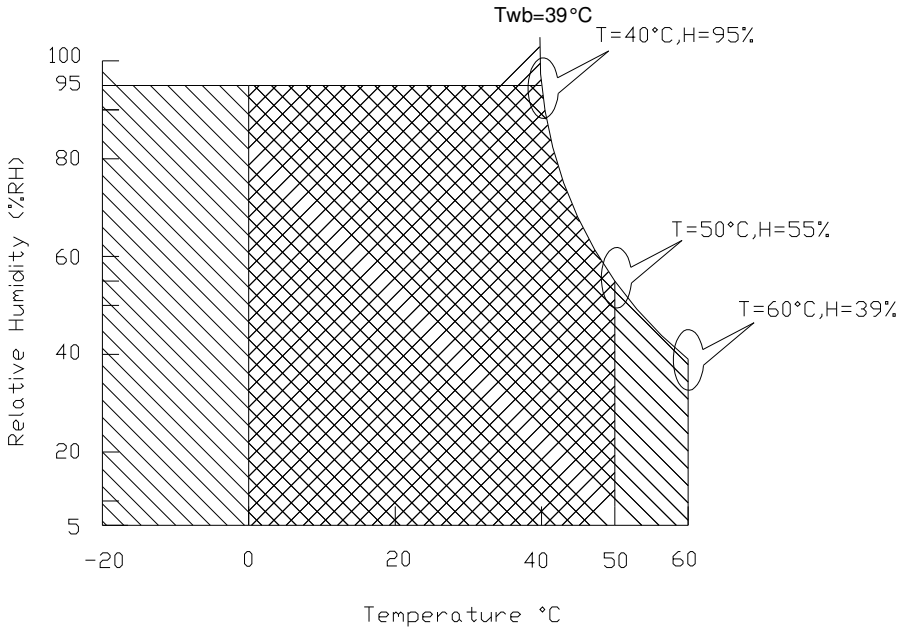
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

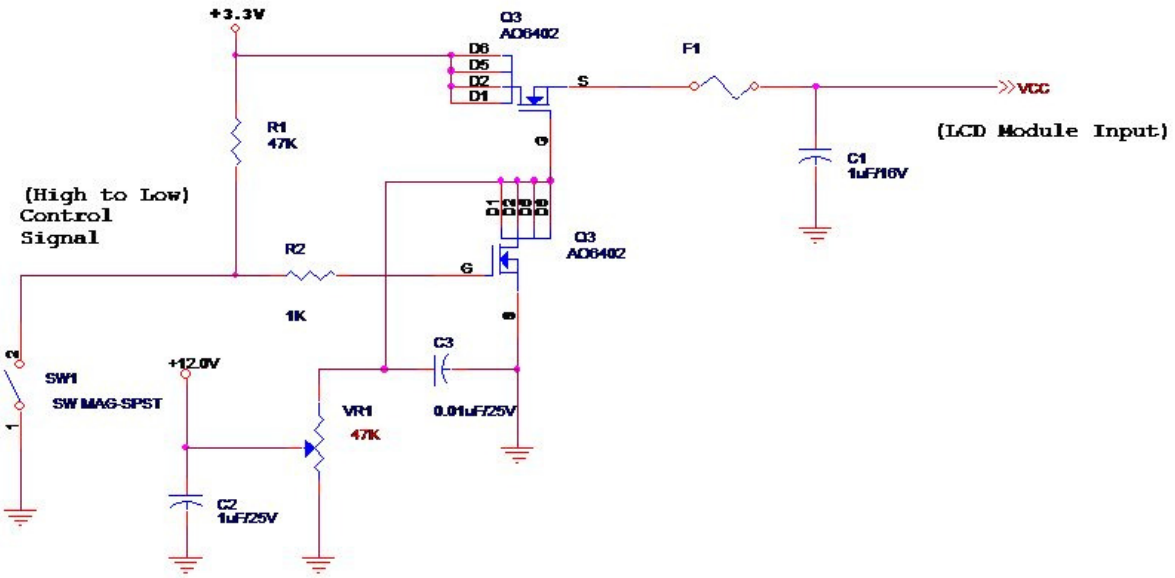
Input power specifications are as follows;

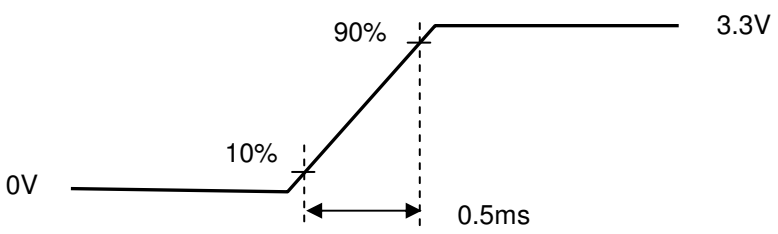
Symble	Parameter	Min	Typ	Max	Unit	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.7	0.8	[Watt	Note 1/2
IDD	IDD Current	-	-	250	[mA]	Note 1/2
IRush	Inrush Current	-	-	1500	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern

Note 2：Typical Measurement Condition: Mosaic Pattern

Note 3：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

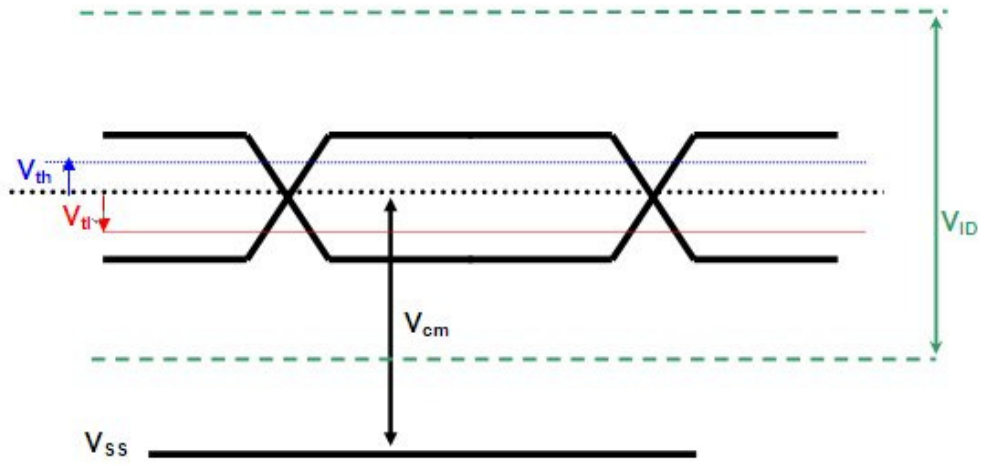
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	2.0	2.1	[Watt]	(Ta=25℃), Note 1 **Type I , V_{in} =12V**
		-	2.4	2.5	[Watt]	(Ta=25℃), Note 1 **Type II , V_{in}=5V**
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous

Note 3: This panel will support lower duty ratio at PWM conditional frequency. The PWM frequency constrain between 100 Hz to 300 Hz and a same typical 200Hz. The duty ratio support from 5% to 100%.

5.2.2 Backlight input signal characteristics

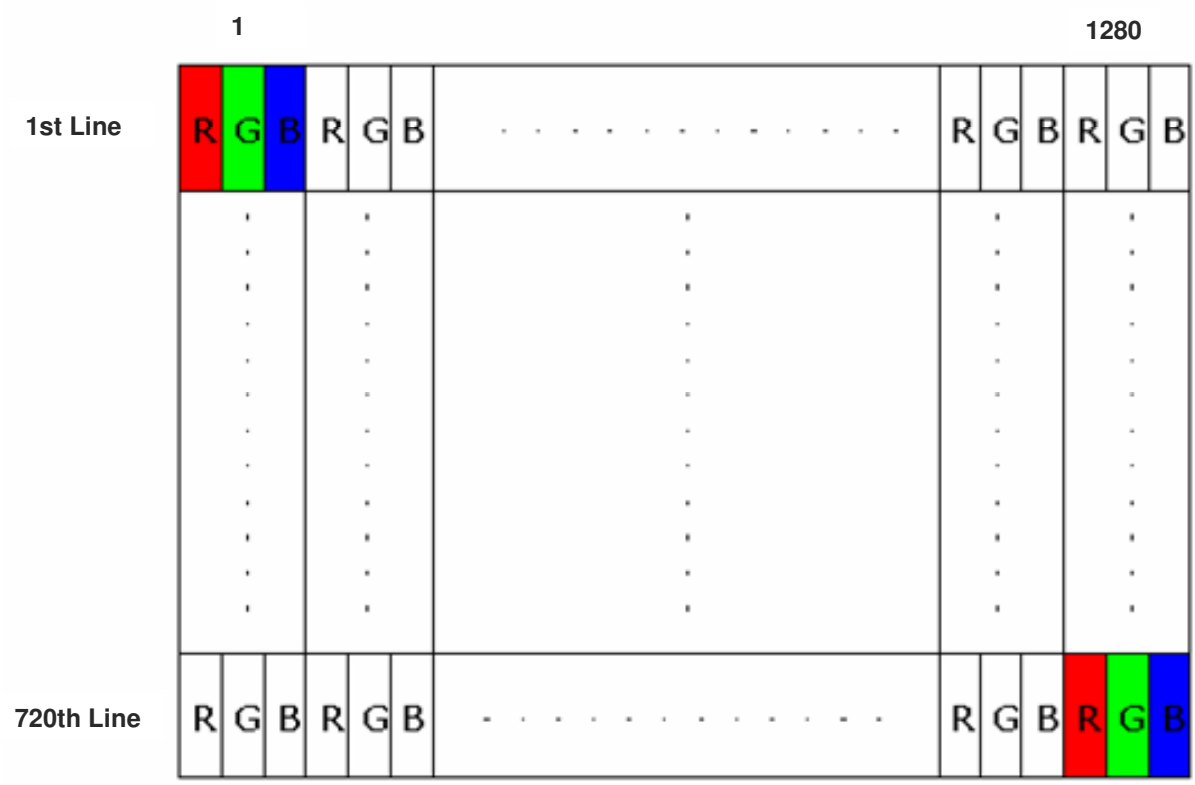
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	**Type I, Note 1**
		4.5	5	5.5	[Volt]	**Type II, Note 1**
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	1K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	PWM Frequency <500 Hz
PWM Duty Ratio	Duty	15	--	100	%	PWM Frequency ≧500 Hz

Note 1: Type I and II is an independent of design parameter. It should be separated from system design.

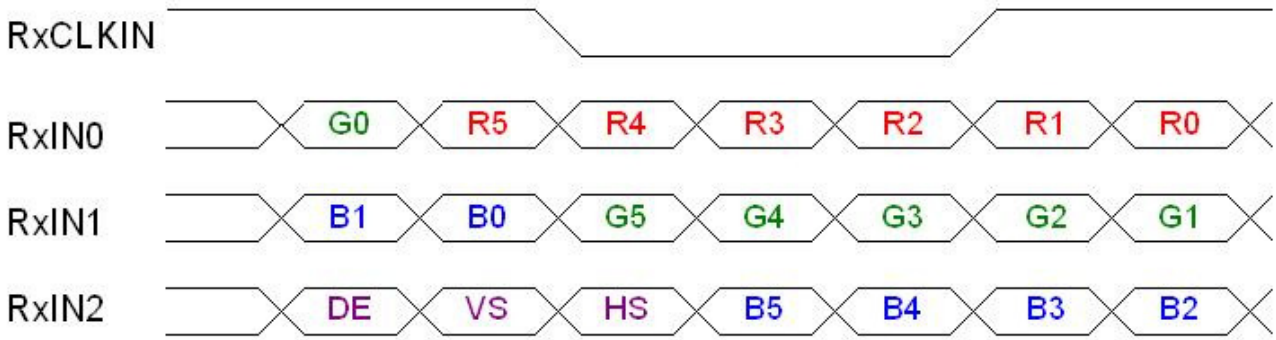
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 54.2MHZ.The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

6.3.2 Pin Assignment

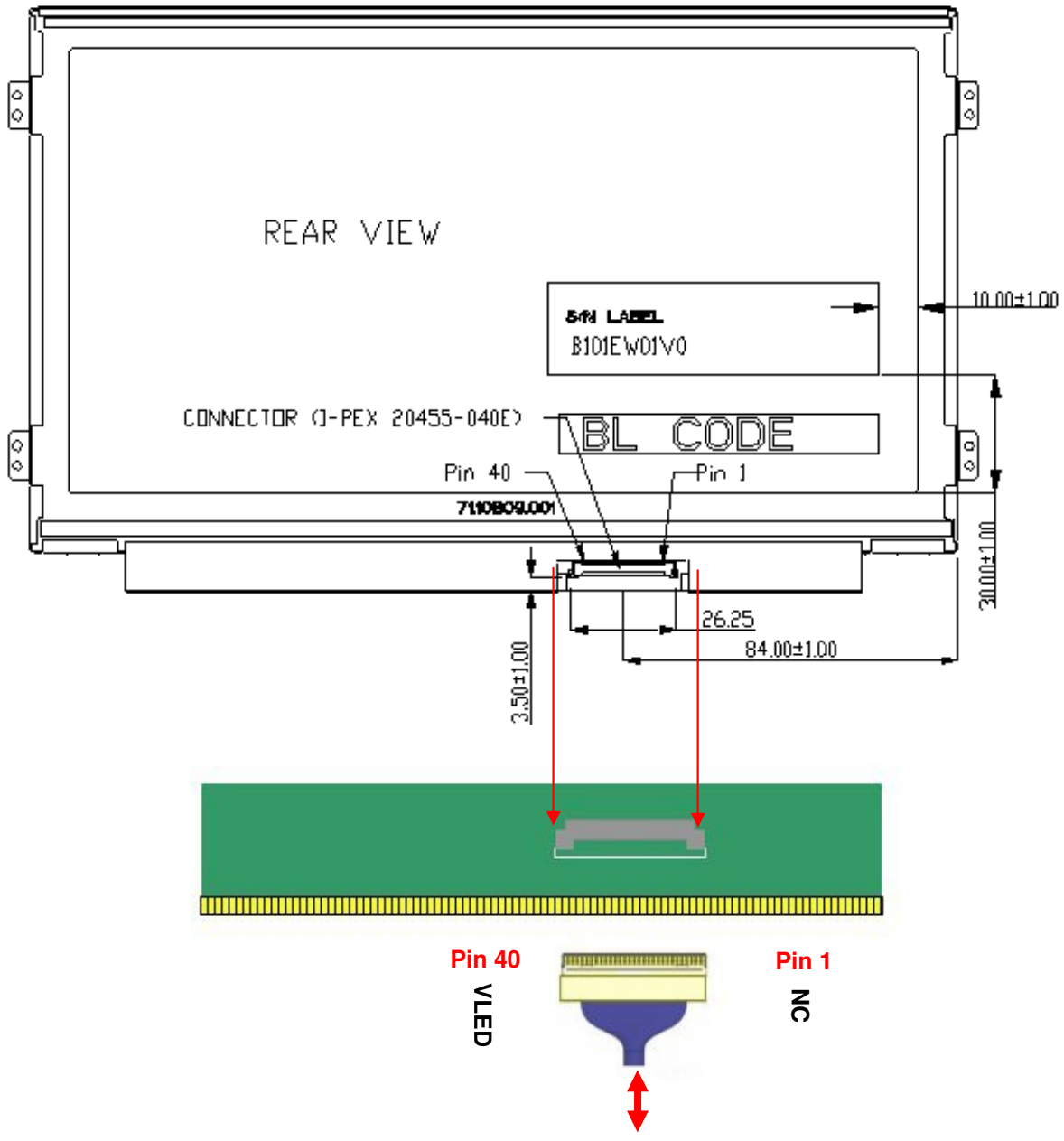
LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	GND	Ground
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connection (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDSdifferential clock input
18	ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)
24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)

30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	System PWM Logic Input Level
36	VLED_EN	LED enable input level
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Note1: Start from right side



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

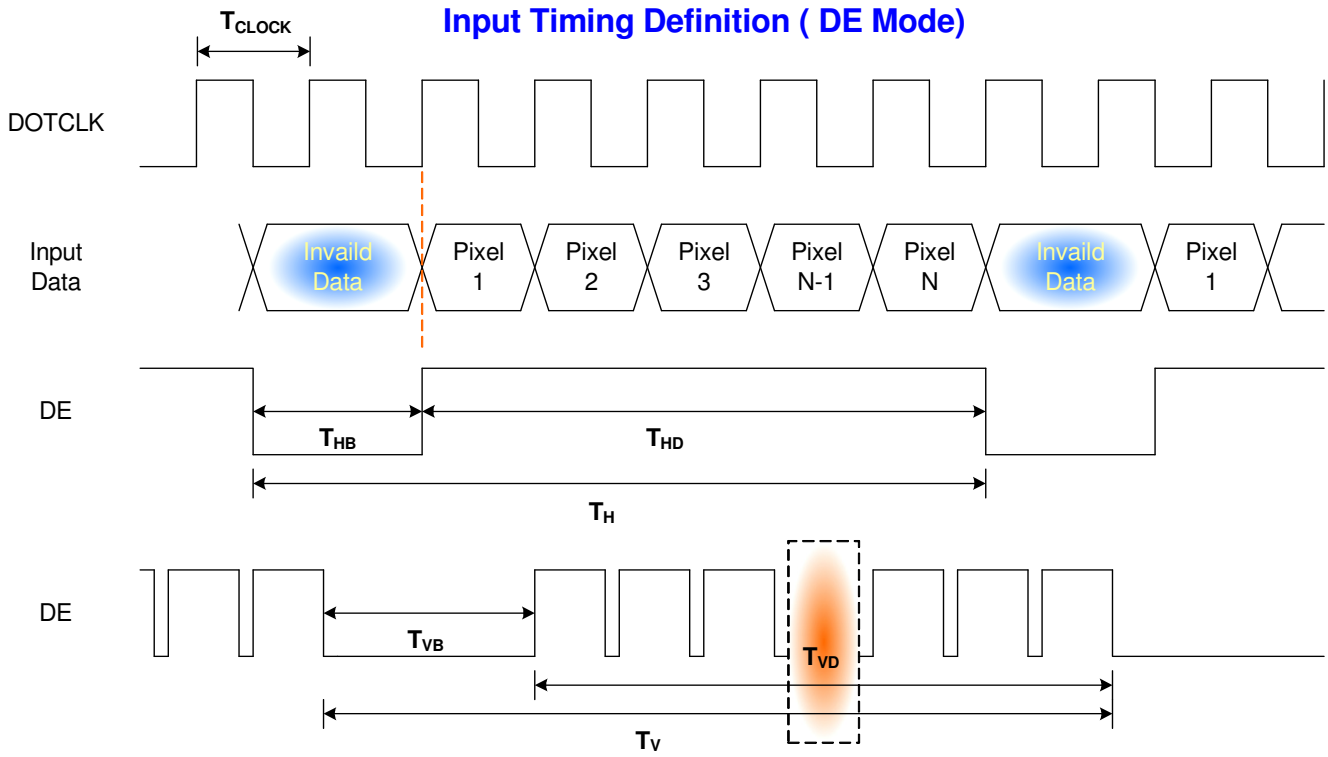
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280 x 720 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60		Hz
Clock frequency		1/ T_{Clock}	57.2	61.5	80	MHz
Vertical Section	Period	T_V	728	736	1023	T_{Line}
	Active	T_{VD}	720	720	720	
	Blanking	T_{VB}	8	16	303	
Horizontal Section	Period	T_H	1310	1408	2047	T_{Clock}
	Active	T_{HD}	1280	1280	1280	
	Blanking	T_{HB}	30	128	767	

Note : DE mode only

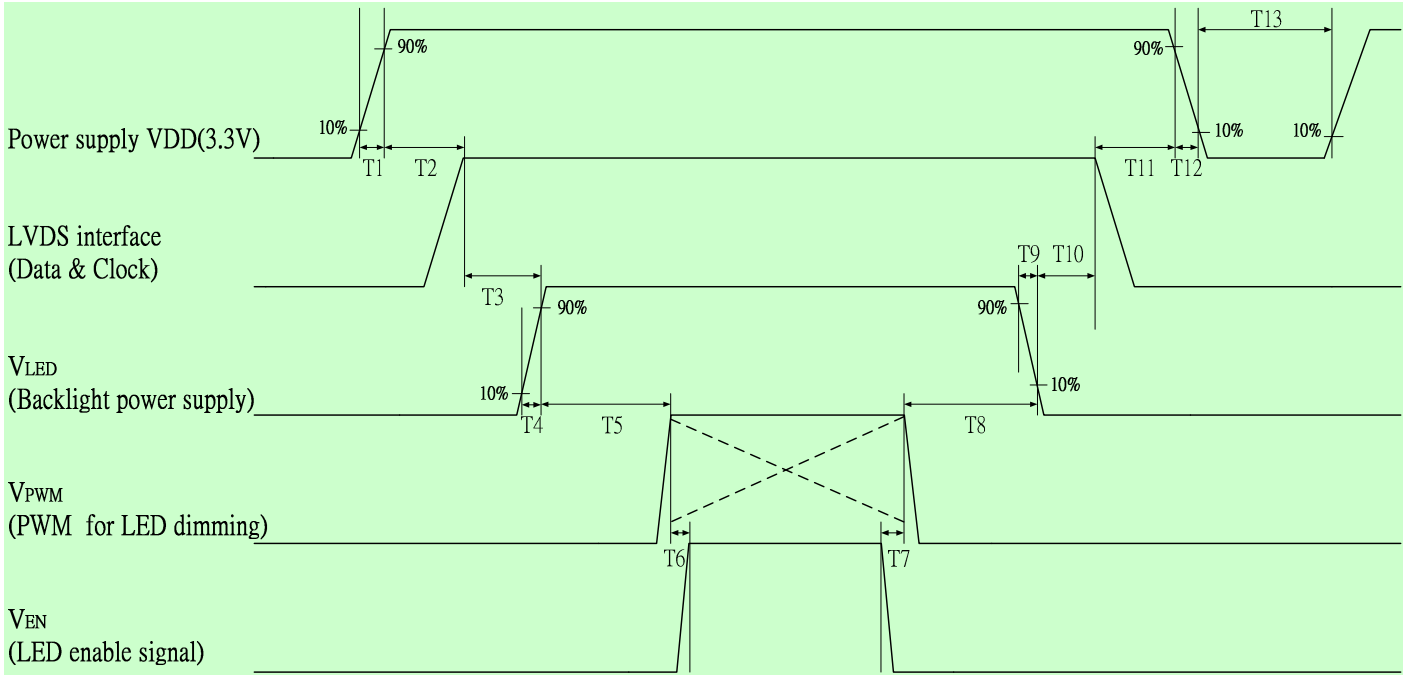
6.4.2 Timing diagram



6.5 Power Sequence

6.5.1 Panel Power Sequence

VDD power and LED on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing				
Parameter	Value			Condition
	Min.(ms)	Typ.(ms)	Max.(ms)	
T1	0.5	-	10	
T2	0	-	50	
T3	200	-	-	
T4	0.5	-	10	
T5	10	-	-	
T6	10	-	-	
T7	0	-	-	
T8	10		200	VLED=6~21V(Type I)
	10	-	-	VLED=5V(type II)
T9	0	-	10	
T10	200	-	-	
T11	0.5	-	50	
T12	0	-	10	
T13	400	-	-	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

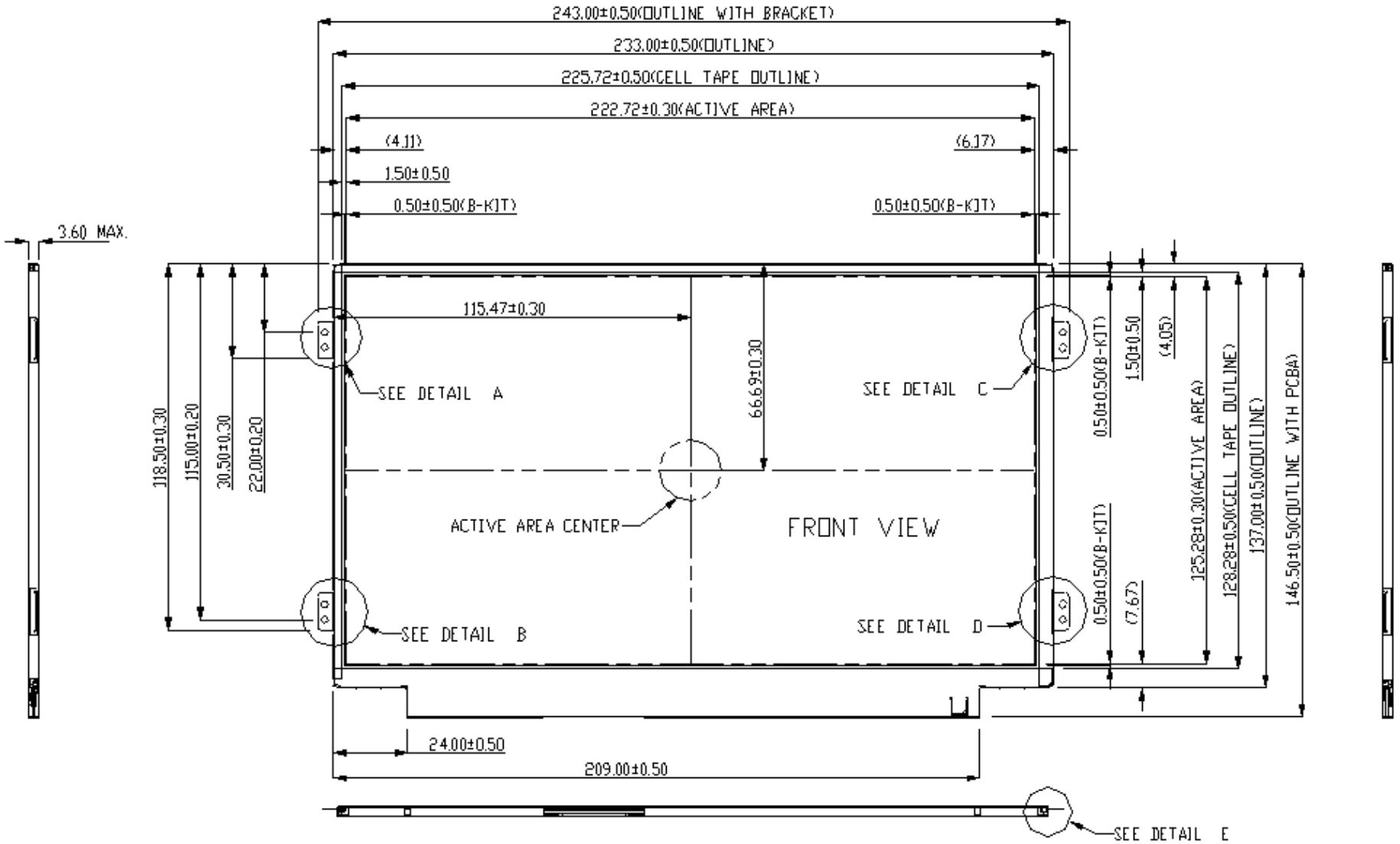
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

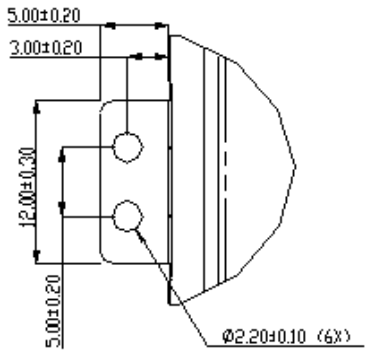
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

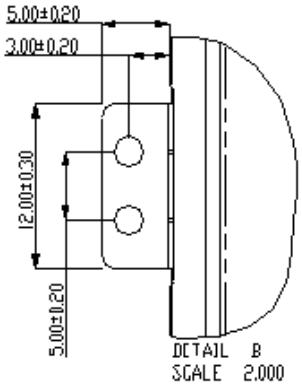
8. Mechanical Characteristics

8.1 LCM Outline Dimension

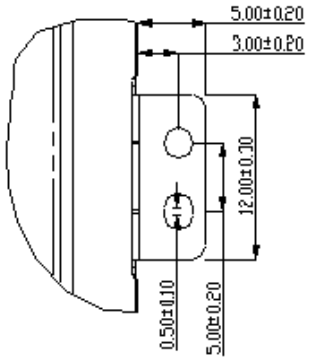




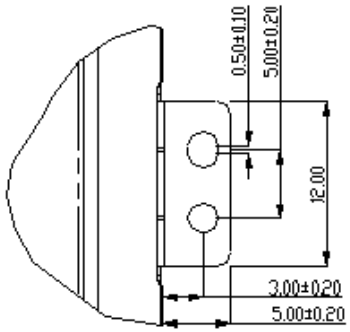
DETAIL A
SCALE 2.000



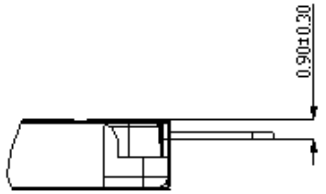
DETAIL B
SCALE 2.000



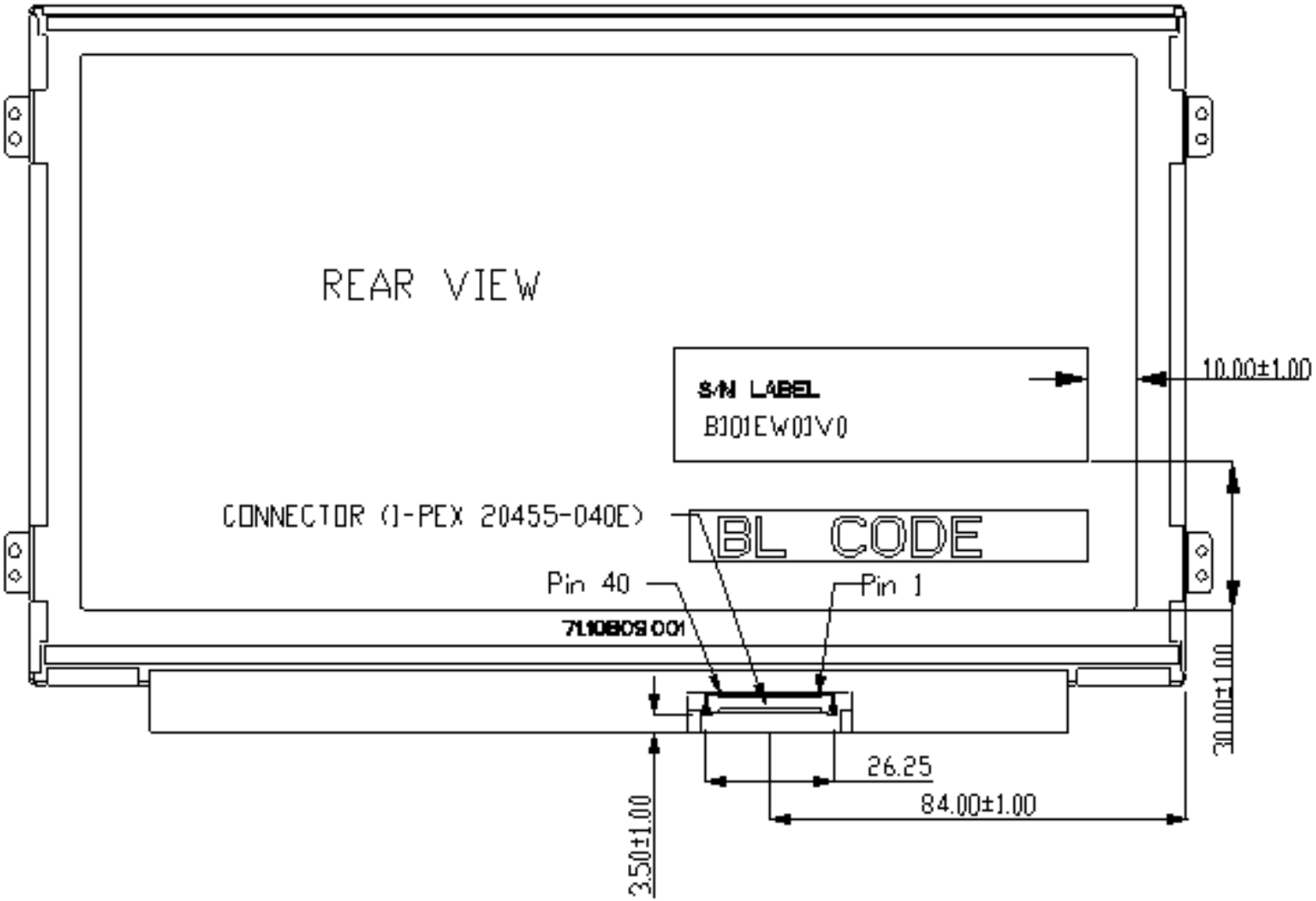
DETAIL C
SCALE 2.000



DETAIL D
SCALE 2.000

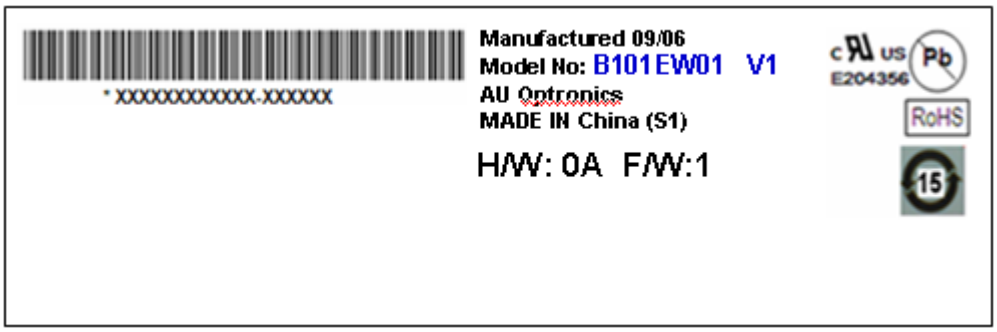


DETAIL E
SCALE 3.000


REAR VIEW
S/N LABEL
B101EW01V0
CONNECTOR (I-PEX 20455-040E)
BL CODE
Pin 40
Pin 1
10.00±1.00
30.00±1.00
26.25
84.00±1.00
3.50±1.00

9. Shipping and Package

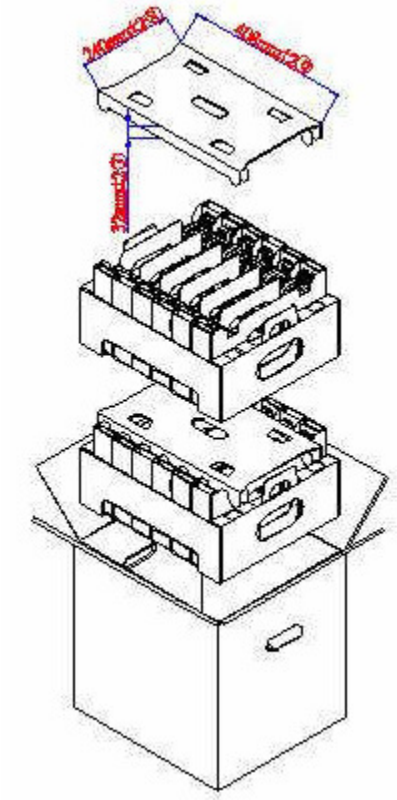
9.1 Shipping Label Format



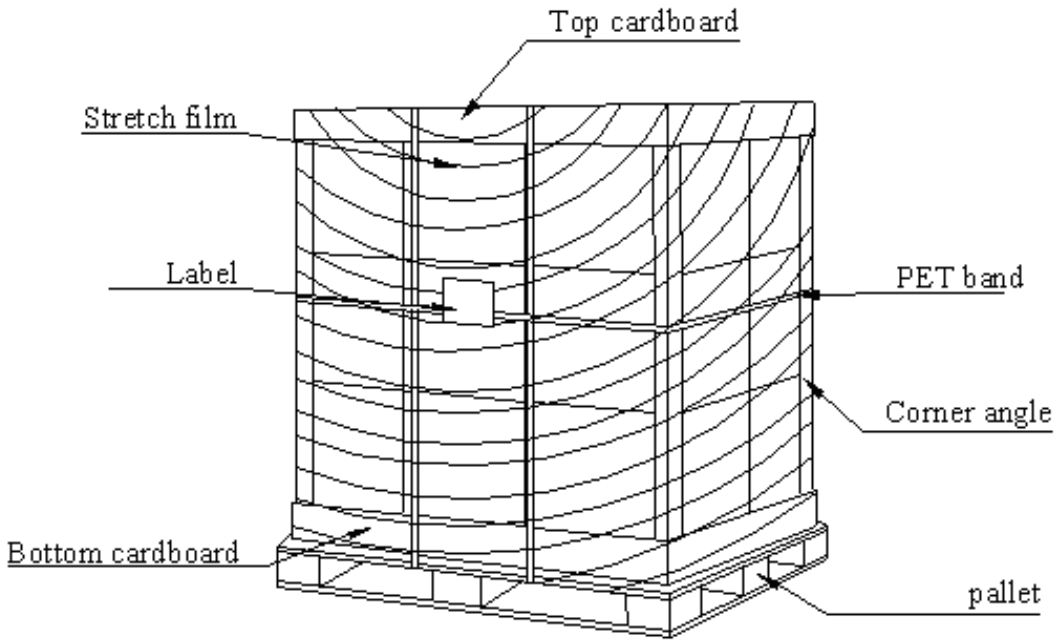
* H/W code control table :

IC Combination		Control Code	H/W
Source	Novatek	OAXXG	OA
Gate	Novatek		

9.2 Carton package



9.3 Shipping package of palletizing sequence



10. Appendix: EDID description

B101EW01 V1 EDID Code

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	D5	11010101	213
0B	hex, LSB first	11	00010001	17
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	13	00010011	19
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80	10000000	128
15	**Max H image size** *(rounded to cm)*	16	00010110	22
16	**Max V image size** *(rounded to cm)*	0D	00001101	13
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010	10
19	Red/green low bits **(Lower 2:2:2:2 bits)**	D1	11010001	209
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	15	00010101	21
1B	Red x **(Upper 8 bits)**	94	10010100	148
1C	Red y/ highER 8 bits	56	01010110	86
1D	Green x	55	01010101	85
1E	Green y	93	10010011	147
1F	Blue x	29	00101001	41
20	Blue y	23	00100011	35
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0

25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	06	00000110	6
37	Pixel Clock/10000 USB	18	00011000	24
38	Horz active **Lower 8bits**	00	00000000	0
39	Horz blanking **Lower 8bits**	70	01110000	112
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	D0	11010000	208
3C	Vertical Blanking **Lower 8bits**	10	00010000	16
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	20	00100000	32
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	DE	11011110	222
43	Vertical Image Size **Lower 8bits**	7D	01111101	125
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0

50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	30	00110000	48
74	Manufacture P/N	31	00110001	49
75	Manufacture P/N	45	01000101	69
76	Manufacture P/N	57	01010111	87
77	Manufacture P/N	30	00110000	48
78	Manufacture P/N	31	00110001	49
79	Manufacture P/N	20	00100000	32
7A	Manufacture P/N	56	01010110	86

7B	Manufacture P/N	31	00110001	49
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	C3	11000011	195